

54  
ok.

FIG. 898  
(Prior Art)

514  
0.1K.

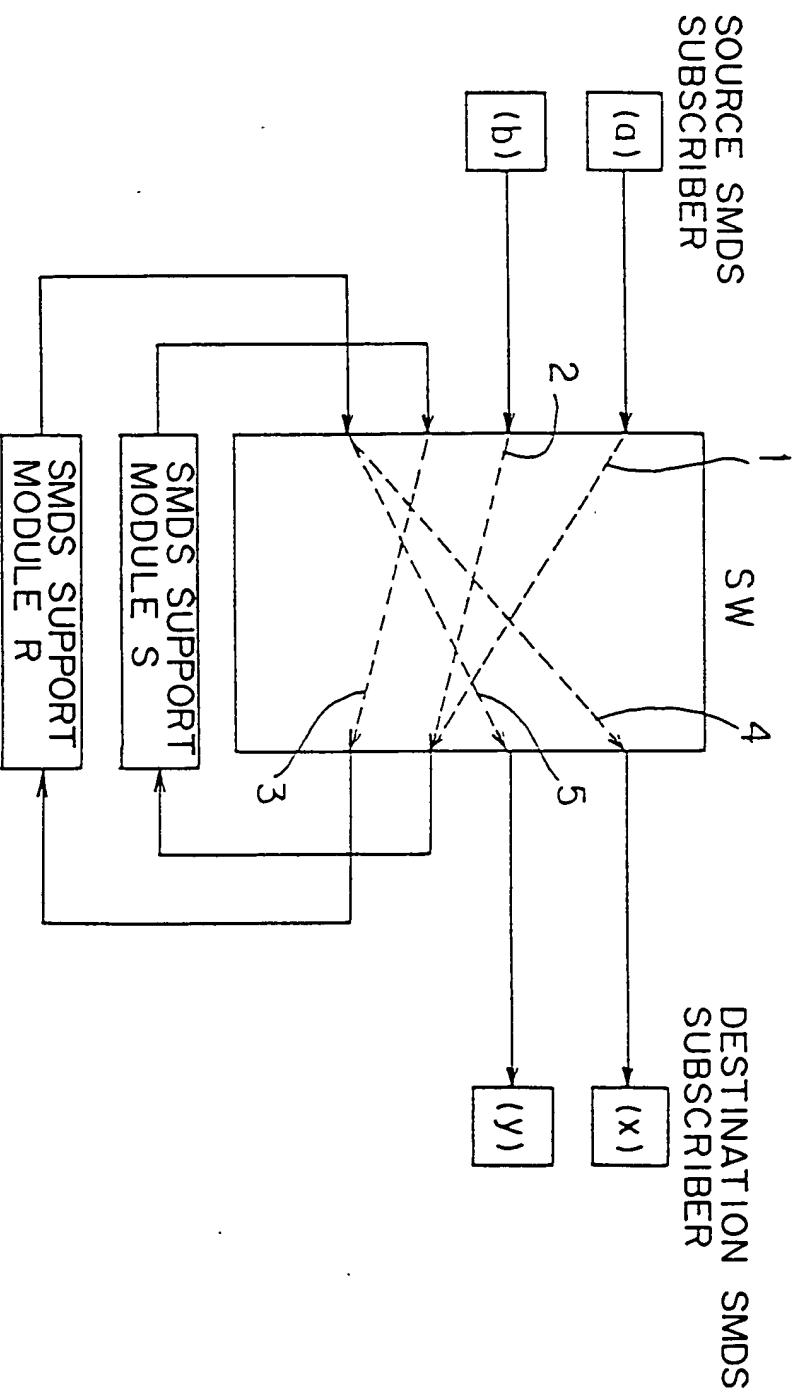
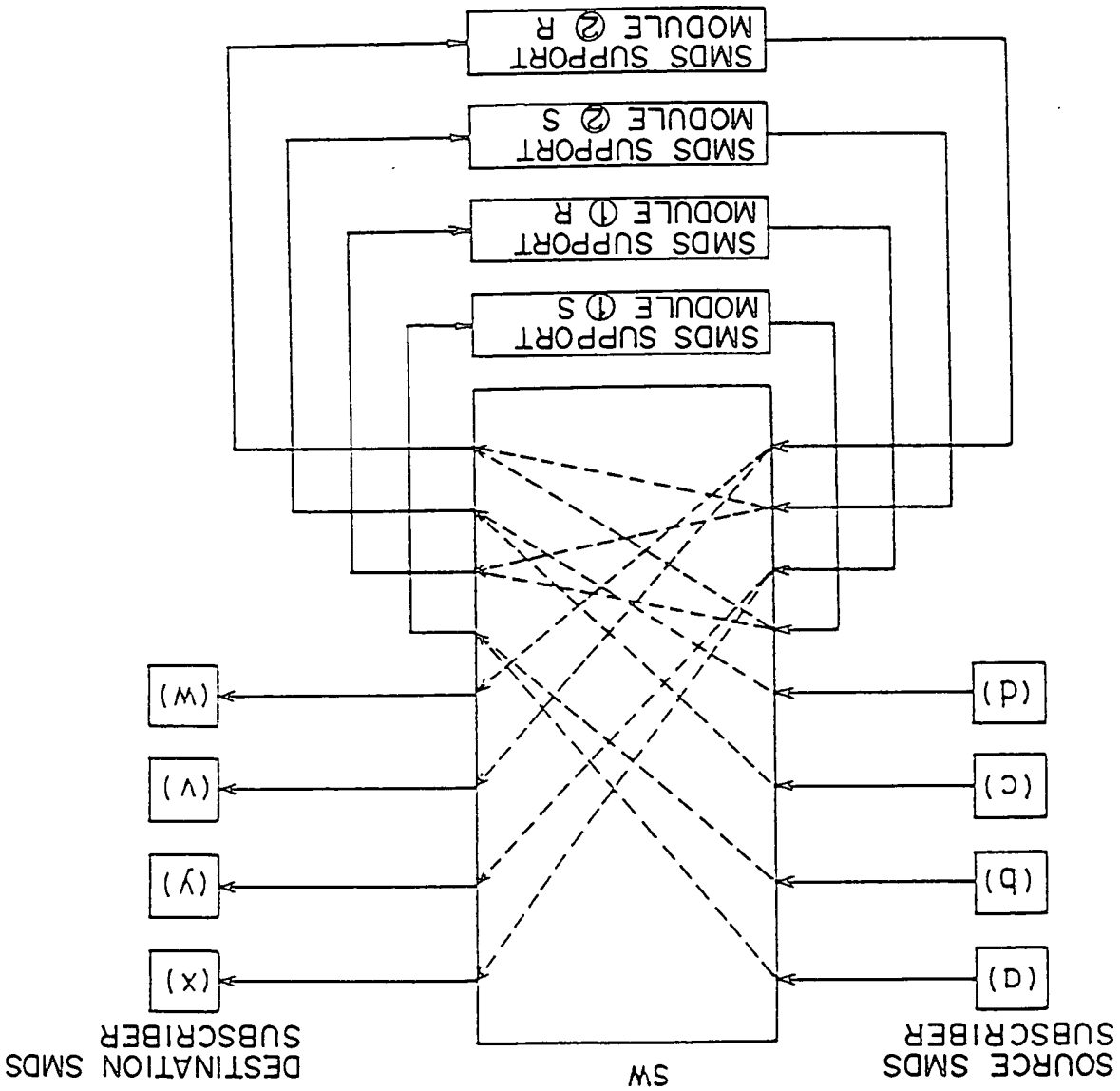


FIG. 899  
(Prior Art)

(Prior Art)

FIG. 900



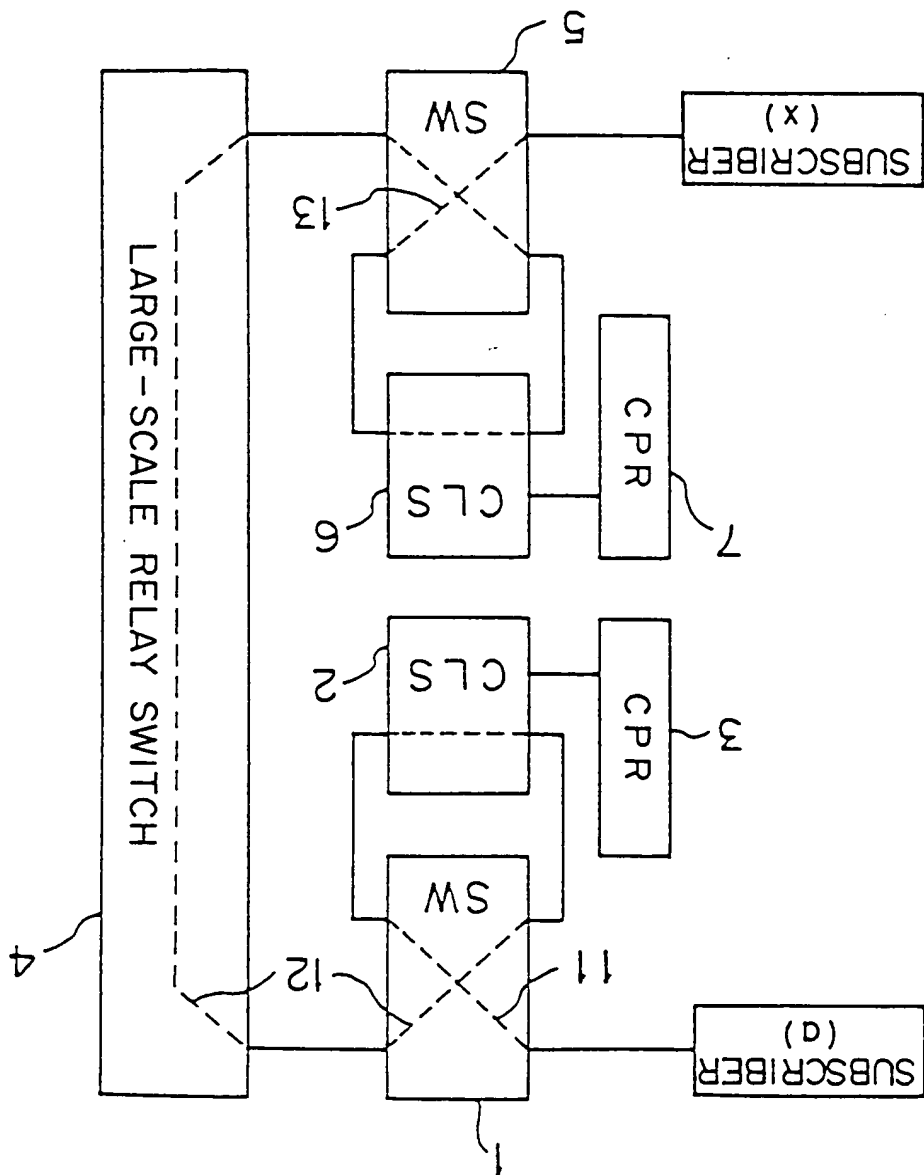


FIG. 901  
(prior art)

SH  
OK.

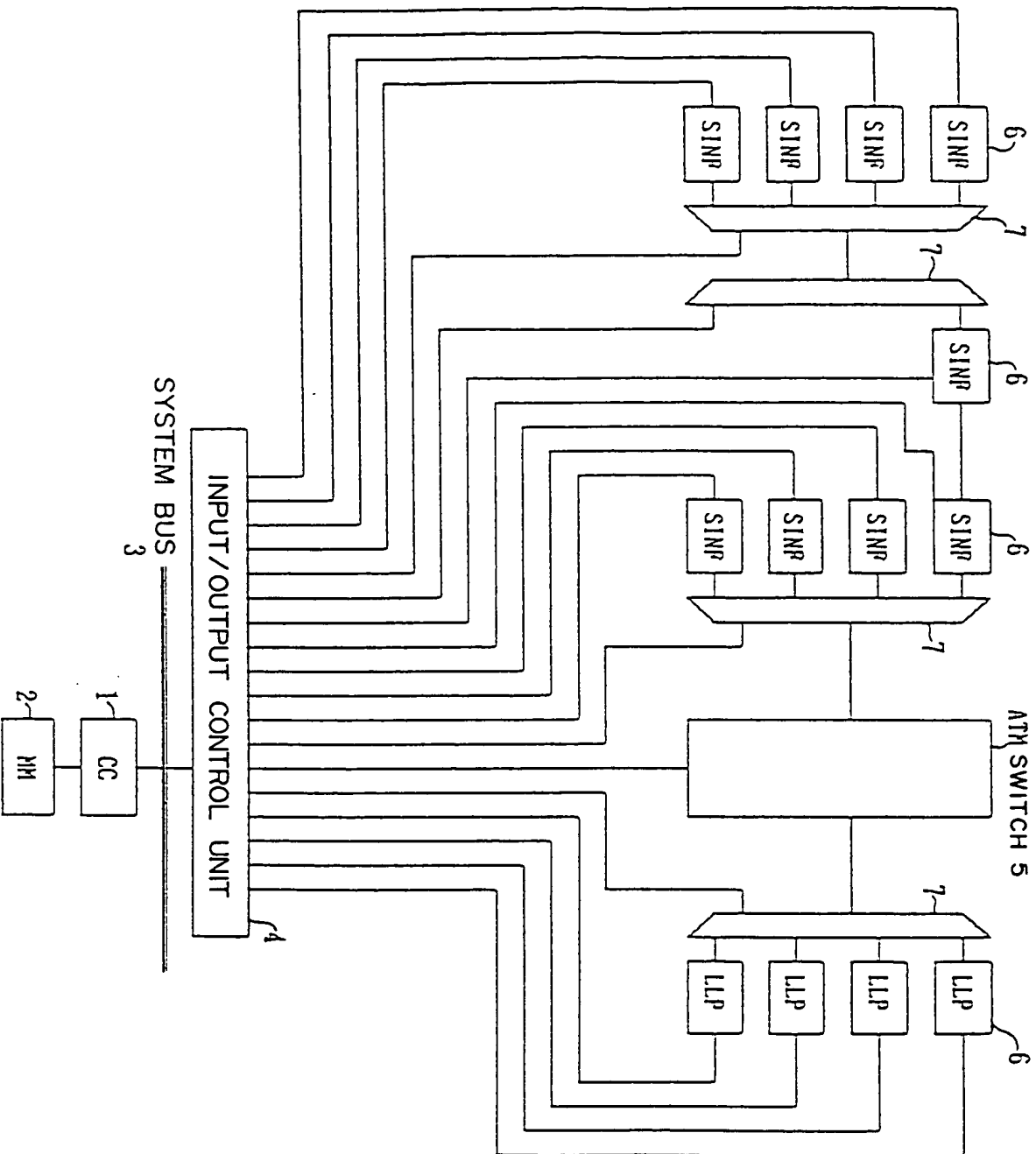


FIG. 902

(Prior Art)

SH  
OK.

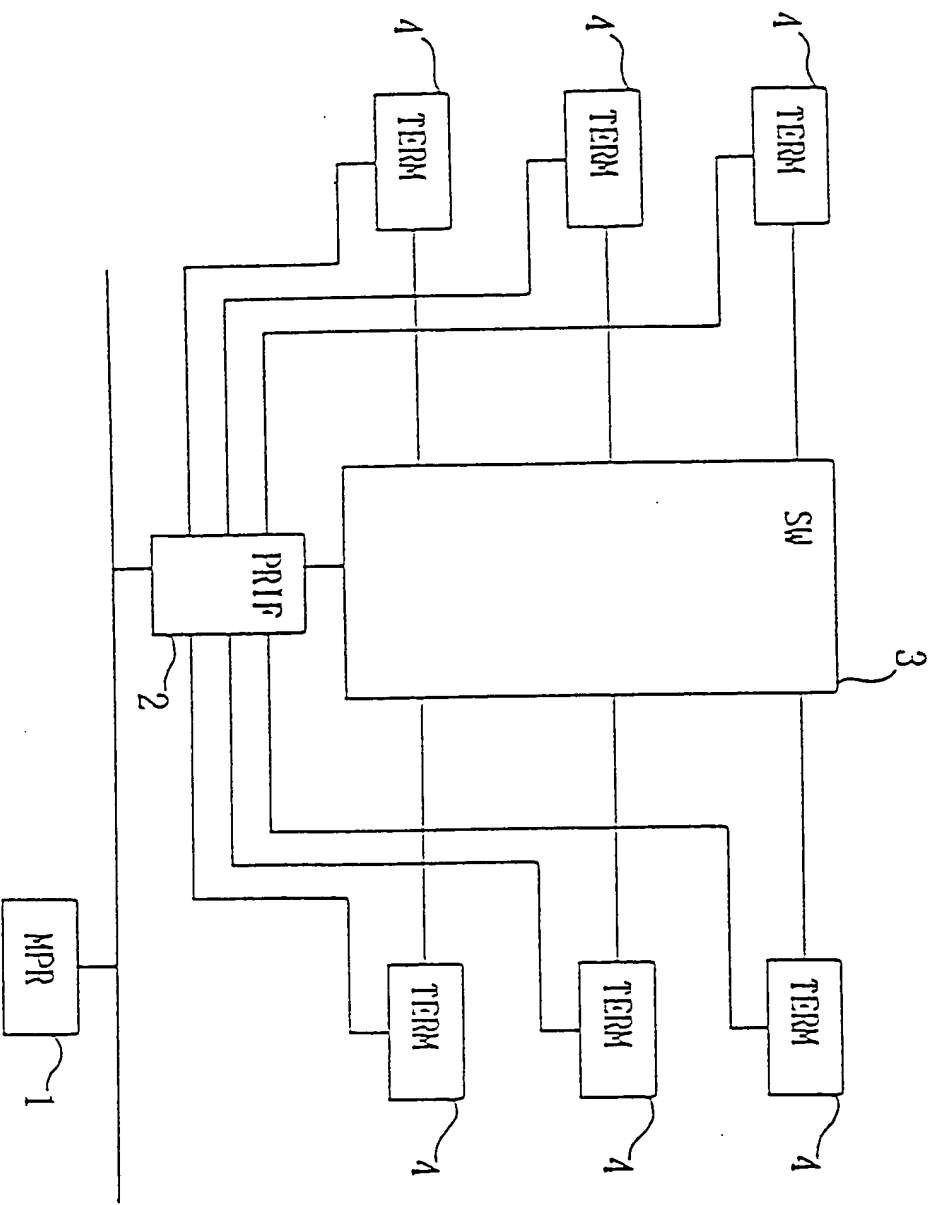
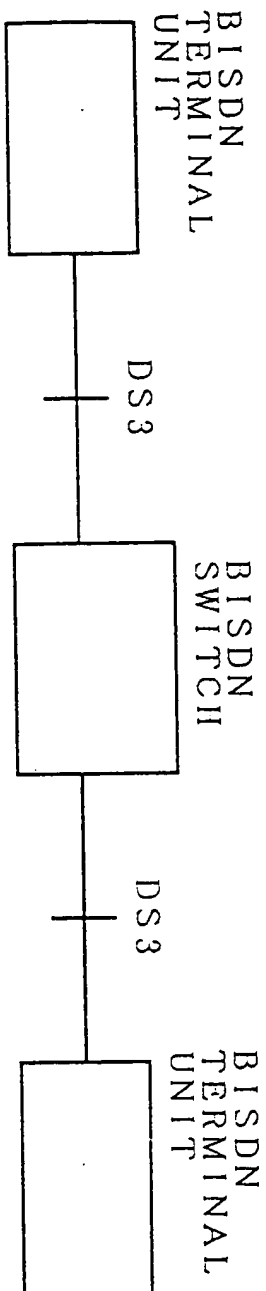


FIG. 903  
(Prior Art)



54  
0.1c

FIG. 904  
(Prior Art)

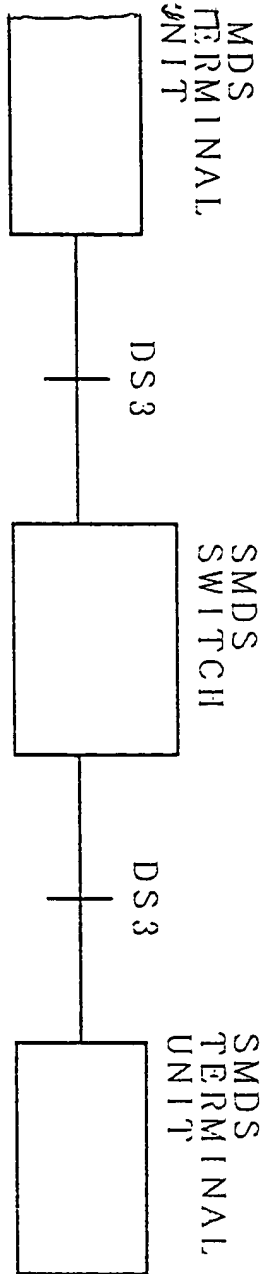


FIG. 905  
(Prior Art)

54  
O.K.



[illegible]

F 0, P 1 : SUBFRAME ALIGNMENT BIT  
M 0, M 1 : MULTIFRAME ALIGNMENT BIT  
P : PARTY INFORMATION BIT  
X : ERROR STATE DESIGNATION BIT  
C (RESERVED)

FIG. 906

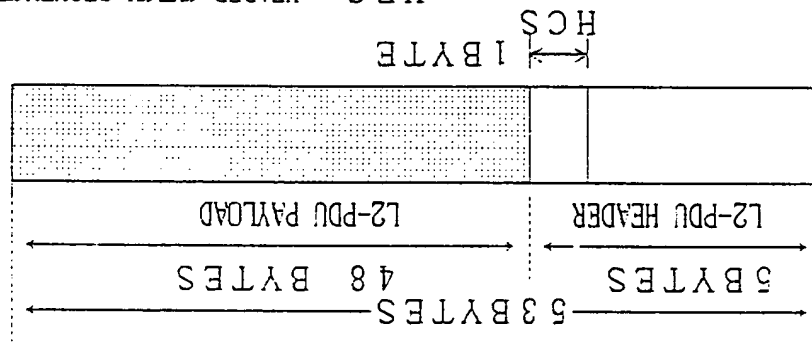
(Prior Art)

(Prior Art)

FIG. 907

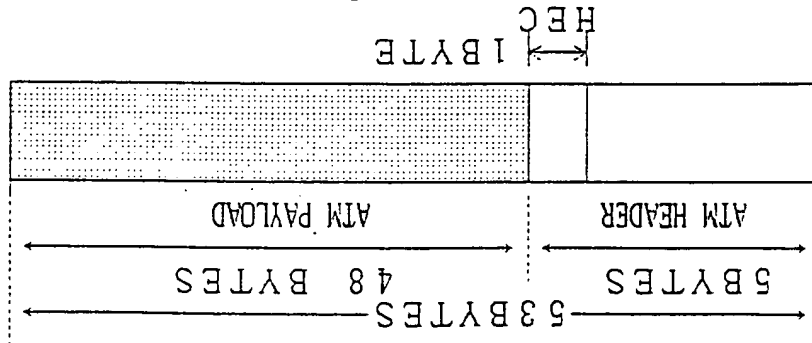
(b) CONFIGURATION OF SMDS CELL

HEC : HEADER CHECK SEQUENCE



(a) CONFIGURATION OF ATM CELL

HEC : HEADER ERROR CONTROL

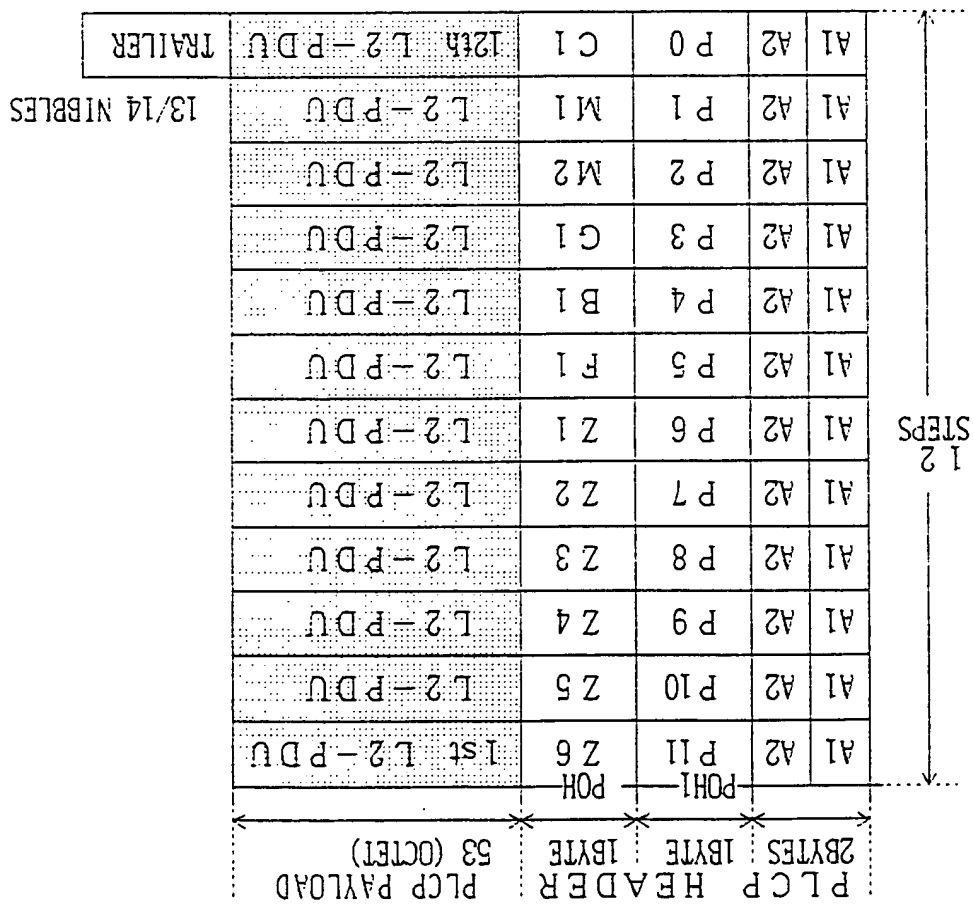


SH  
OK

(Prior Art)

FIG. 908

A1, A2 : FRAME ALIGNMENT  
 POH1 (P11~P0) : PATH OVERHEAD IDENTIFIER OCTET  
 POH : PATH OVERHEAD OCTET  
 Z6~Z1 : GROSS OCTET  
 F1 : PLCP PATH USER CHANNEL  
 B1 : BIT INTERVAL PARITY 8  
 C1 : PLCP PATH STATUS  
 M1~M2 : SIP LEVEL 1 CONTROL INFORMATION  
 C1 : CYCLE STUFF COUNTER



SH  
OK.

ITEM		BIT PATTERN	REMARKS
C1	CYCLE STUFF COUNTER	11111111	TL IS REPRESENTED BY 4 TYPES OF C1 AS SHOWN BELOW BECAUSE TRAILER LENGTH TL PERIODICALLY CHANGES IN DS3 PLCP FRAME.
		00000000	
		01100110	
		10011001	
TRAILER		1100	LENGTH DEPENDS ON C1 BYTE VALUE.

54  
 o.k.  
 FIG. 909  
 (Prior Art)

SH  
o.k.

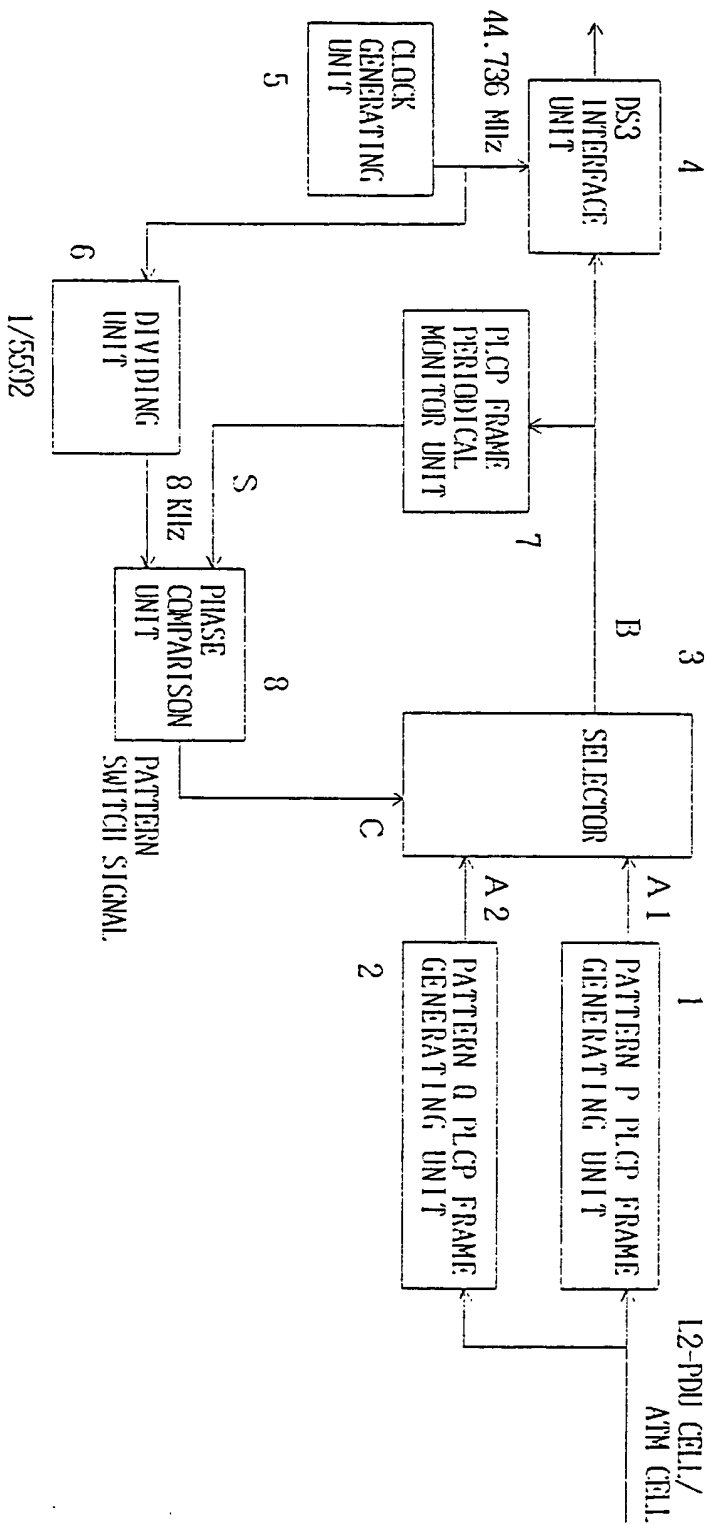


FIG. 910

(Prior Art)

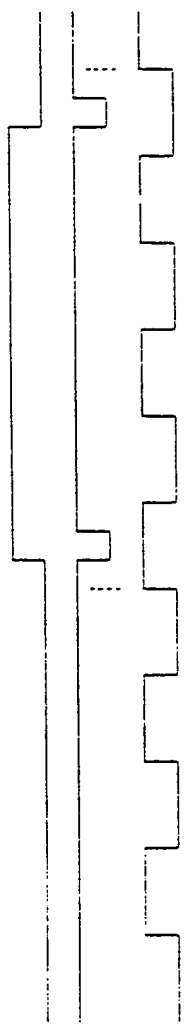
8 KHz

S

C

PATTERN

B



Q			P			Q		

FIRST PLCP FRAME	SECOND PLCP FRAME	THIRD PLCP FRAME	FIRST PLCP FRAME	SECOND PLCP FRAME	THIRD PLCP FRAME
------------------------	-------------------------	------------------------	------------------------	-------------------------	------------------------

SH  
OK.

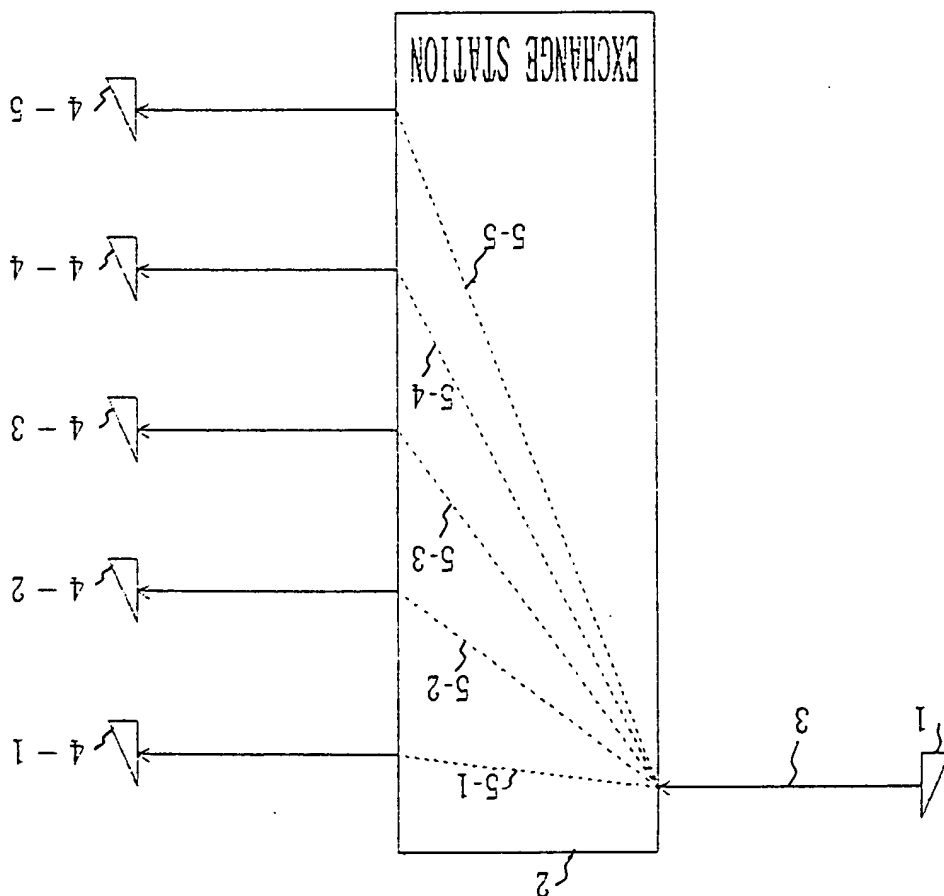
FIG. 911

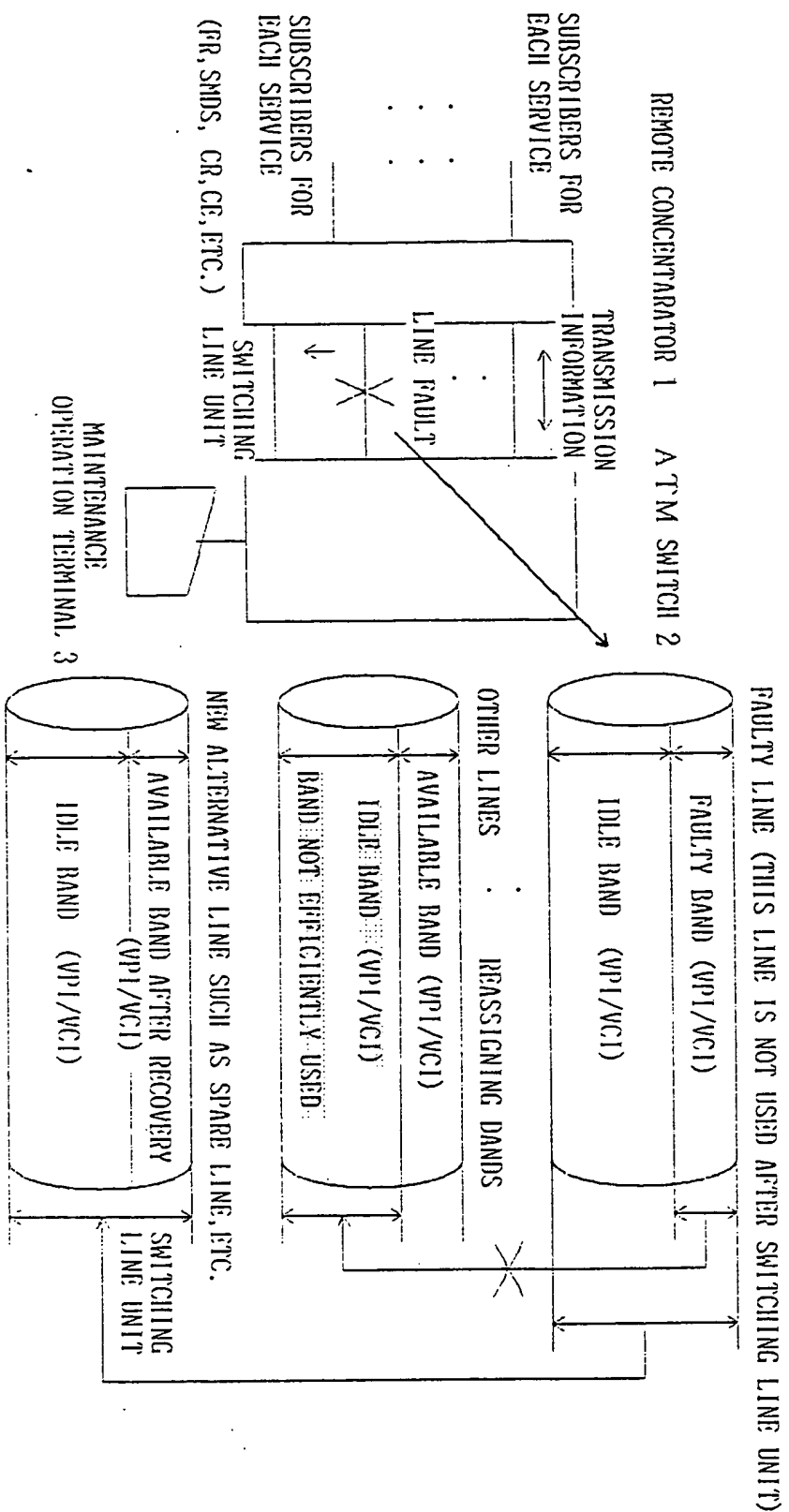
(Prior Art)

SH  
0.1c.

(Prior Art)

FIG. 912





SH  
ok.

FIG. 913

(Prior Art)